Measurement of Circuit Parasitics of a 200kW SiC based Stack

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***Abstract*— Converters with high power density are becoming necessary in applications such as traction inverters and electric vehicles, where the inverter stage must process power in the range of a few hundred kilowatts. As the inverters are often hard-switched, SiC power modules can enable high power density due to superior switching, conduction loss, and thermal performance. However, due to the fast switching transients of SiC MOSFETs, circuit parasitics can significantly impact the switching dynamics resulting in prolonged oscillation, high device stress, and crosstalk and EMI-related issues. So, estimation of circuit parasitic is essential for optimal gate and power circuit layout design. The experimental measurement-based parasitic estimation technique is superior to the electromagnetic simulation-based approach when the internal geometry of the power module is unknown. This paper presents a systematic approach to estimating parasitic inductances of a 200 kW SiC-based stack. The accuracy of this proposed method is verified through experiment and electromagnetic simulation with the help of ANSYS Q3D Extractor.**

***Index Terms*—SiC Stack, Parasitic Inductance Measurement, Ansys Q3D Extractor.**

I. Introduction

SiC MOSFETs are rapidly replacing Si IGBTs in power electronic converters due to their superior switching, conduction loss, and thermal performance [1]. Due to reduced power loss, converters with SiC MOSFETs can operate at higher switching frequencies, thus enabling smaller filter sizes and high-power densities. To cater to applications such as electric vehicles and electric aircraft, high-power converters with power ratings of a few hundred kW are required, and high-current (120-760A) SiC power modules are often preferred in these applications [1], [2].

Due to fast switching transients (high $(dv/dt$ and $(di/dt))$, the switching dynamics of SiC MOSFETs are sensitive to circuit parasitics. This may lead to high device stress, sustained oscillations, EMI-related issues, crosstalk, etc, which are well-known side effects of these parasitics [3]. Thus, the accurate estimation of these circuit parasitics is vital for the optimal power converter design.

Extraction of parasitic inductance has been given considerable attention in the existing literature [4], [6], and it can be of two types: (a) simulation [4], [5] and (b) experimental. Electromagnetic simulation-based parasitic extraction is accurate. However, they require expensive software packages, long computation time, and domain knowledge and may have convergence issues. Moreover, details of the internal structure of the packaged power module are required for simulation, which may not be available to a design engineer [3]. In such a case, measurement becomes the only option to estimate the circuit parasitics. Measurement-based approaches can be of two types: (a) time domain reflectometry (TDR) and (b) frequency response analysis (FRA). TDR measurements require expensive equipment and lack accuracy when the characteristic impedance of the device under test deviates from 50Ω [7]. On the other hand, FRA-based one-port or two-port measurements requires specially designed PCBs and careful calibration. Also, the measurements may become erroneous at higher frequencies [8]. In addition to these, alternate equivalent circuit-based measurement techniques can be used to extract circuit parasitics. Compared to the previous two techniques, no specialized equipment is needed, and the measurements are done with the oscilloscope and voltage/current probes, routinely used for converter development and testing [9]. This technique was used in [3] to estimate the various parasitic inductances, including the dc bus, which was considered a single lumped inductance.

This paper presents an experimental measurement technique based on the equivalent circuit approach to extract the circuit parasitic inductances. Instead of considering the dc bus inductance to be lumped, detailed modelling of the dc bus is considered. Individual extraction of these parasitic inductances is essential for optimal gate resistance and snubber circuit design selection. Two simple tests are proposed to extract these parasitic inductances. The proposed technique requires an oscilloscope, voltage and current probes, and no other spe-

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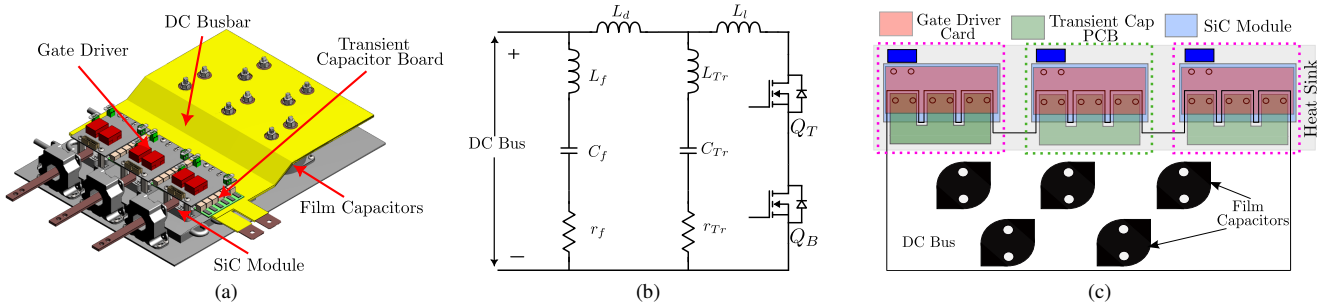

Fig. 1. (a) 200 kW SiC based Stack. (b) Equivalent Circuit for Parasitic Extraction. (c) Top-view of 200 kW SiC based Stack.

cialized equipment. The proposed experimental measurement method is validated through experiments and electromagnetic simulation in ANSYS Q3D Extractor.

The paper's organisation is as follows: Section II presents the system description and specifications. The methodology for parasitic inductance extraction is discussed in Section III. Experimental and simulation results are elaborated in Section IV and V, respectively. Finally, the paper is concluded in Section VI.

TABLE I
RATINGS OF SIC STACK

P	DC Bus Voltage	Output Voltage	f_o	f_s
200 kW	800 ±5% V	230 ±10% V	50 Hz	20-50 kHz

TABLE II
GIVEN PARAMETERS

C_f	C_{Tr}	Ron
350 μF	0.22 μF	3.1 mΩ

II. SYSTEM DESCRIPTION

A 3-D model of the developed 200kW liquid-cooled stack is given in Fig. 1a. 1200V, 805A SiC MOSFET half-bridge modules from Microsemi are used. The total power loss of each half-bridge module is estimated to be around 1.2kW. A cold plate is placed underneath the module for efficient heat extraction. Each module's DC+ and DC- terminals are connected to the DC bus film capacitors through a laminated bus bar. Five 1200V, 70uF (944U700K122AB) film capacitors are placed to get a cumulative DC bus capacitance of 350uF. High-frequency RC snubber circuits are placed close to each module to reduce the high-frequency commutation loop inductance. RC snubber capacitor board consists of MLCC ceramic capacitor (CKC33C443KJGLCAUTO) and thick film SMD resistor. Gate driver cards are also placed individually for each half-bridge module to optimize the gate loop inductance. Sine triangle or space vector modulation is a common modulation technique for three-phase active front-end converters. In any of these modulation techniques, only a single half-bridge takes part in switching transient and devices of the other two bridges will be clamped to V_{dc} or ground. So, the DC bus and the device at high frequency can be modelled as the equivalent circuit given in Fig. 1b. C_f, L_f, r_f represent the cumulative capacitance, equivalent series inductance (ESL), and resistance (ESR) of the film capacitors, respectively. L_d is the parasitic inductance of the DC bus. L_l represents the stray inductance of the bridge. C_{tr}, L_{tr}, r_{tr} represent the cumulative values of transient capacitance, parasitic inductance, and parasitic resistance of the transient capacitor board. The ratings of the overall stack are given in Table I. The values of known parameters are given in Table II. Here, R_{on} represents the on-state resistance of the device.

III. PARASITIC EXTRACTION

The top view of the stack is shown in Fig. 1c. It can be observed that the parasitic inductances seen by the side modules (highlighted in pink in Fig. 1c) are similar due to the symmetric structure, and the parasitic inductances seen by the middle module (highlighted in green in Fig. 1c) are different from the side modules. So, it is required to extract the parasitic inductances for two different cases, considering the middle and any one of the side modules separately. The following tests are conducted to estimate the values of L_l, L_d, L_{Tr}, for given values of C_f, C_d, R_{on}.

A. Test-I

In Test-I, the transient capacitor board is removed from the setup (see Fig. 2a). The SiC MOSFET, Q_T, is kept in on-state by applying a positive gate voltage V_{GG}. So, it can be modelled by its on-state resistance (R_{on}). Initially, Q_B is off, and a small DC bus voltage $V_{dc(test)}$ is applied across the film capacitor. So, Q_B blocks $V_{dc(test)}$. A positive gate pulse with time duration T_{test} is applied to Q_B. Note: the value of T_{test} is chosen to be sufficiently large compared to the settling time of the gate-source voltage of Q_B. Thus, Q_B can also be approximately modelled as R_{on} for most of this test's duration. The final equivalent circuit for Test-I is also shown in Fig. 2a, which forms a second-order RLC circuit with $R_{eq} = 2 * R_{on} + r_f + r_d$, $L_{eq} = L_l + L_d + L_{Tr}$. Here, r_d represents the high-frequency parasitic resistance in the power loop. For a practical values of C_f, the response i_{dc} is over-damped and it can be expressed as (1), where $S_{1,2}$ is expressed in (2), which can be solved with the initial conditions $i_{dc}(0) = 0$ and $V_f(0) = V_{dc(test)}$. The parameters R_{eq} and L_{eq} can be obtained by curve fitting the experimentally obtained i_{dc} curve using the above expression.

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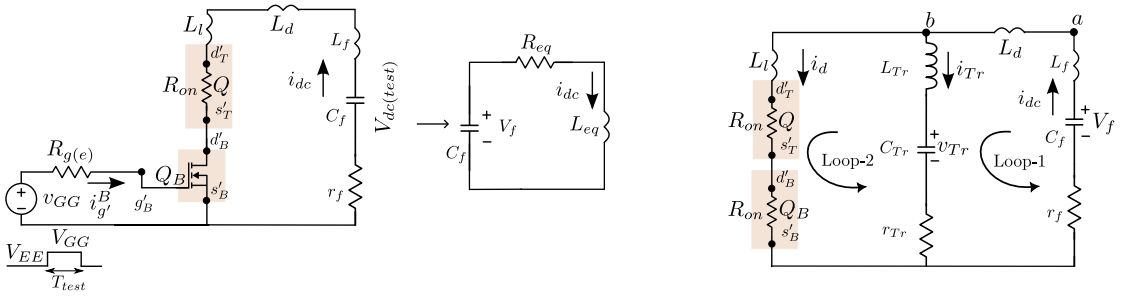

Fig. 2. (a) Equivalent Circuit for Test-I. (c) Equivalent Circuit for Test-II.

$$i_{dc}(t) = (A_1 e^{s_1 t} + A_2 e^{s_2 t}) C_f V_{dc(test)} \tag{1}$$

$$S_{1,2} = -\frac{R_{eq}}{2L_{eq}} \pm \sqrt{(\frac{R_{eq}}{2L_{eq}})^2 - \frac{1}{L_{eq}C_f}} \tag{2}$$

B. Test-II

For Test-II, the circuit configuration similar to Test-I is used. The transient capacitor board is placed across the module's DC positive and negative terminals. $V_{dc(test)}$ is applied across the film capacitors, and Q_T is gated. Initially, Q_B is blocking $V_{dc(test)}$. Q_B is turned on for a time period of T_{test}, and can be modeled as R_{on}. Fig. 2a represents the equivalent circuit of Test-II. The initial capacitor voltage is represented as, $V_f(0) = V_{dc(test)}$. Initially, the switching current is supplied by the transient capacitance C_{Tr}. Thus, C_{Tr} forms a damped tank with $L_l + L_{Tr}$, and the current i_d shows a high-frequency component on top of the over-damped RLC power loop formed by R_{eq}, L_{eq}, C_f.

By applying KVL in Loop-1, (3) is obtained, where $L_T = L_d + L_f$. Similarly, (4) is obtained by applying KVL in Loop-2, and (5) and (6) are obtained by applying KCL at nodes (a, b), respectively. (3)-(6) represents a 4^{th} order system, which governs the dynamics of Test-II. However, obtaining the explicit expression for the device current is difficult to obtain, due to the system's complexity. Hence, an optimization procedure is used to obtain parasitic inductances.

$$V_f = i_{dc} r_f + L_T \frac{di_{dc}}{dt} + L_{Tr} \frac{di_{Tr}}{dt} + v_{Tr} \tag{3}$$

$$v_{Tr} = -L_{Tr} \frac{di_{Tr}}{dt} + L_l \frac{di_d}{dt} + 2 i_d R_{on} \tag{4}$$

$$i_{dc} = -C_f \frac{dV_f}{dt} \tag{5}$$

$$i_{Tr} = -C_{Tr} \frac{dv_{Tr}}{dt} \tag{6}$$

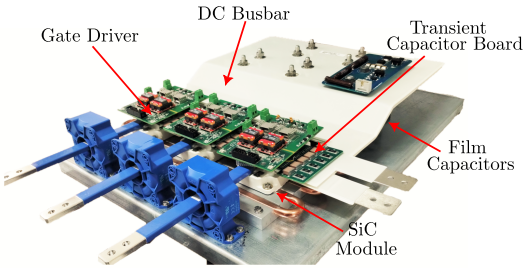

Fig. 3. Experimental setup of 200 kW Stack.

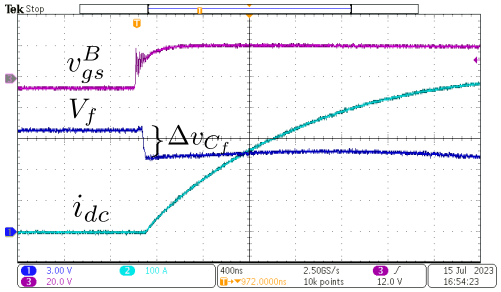

Fig. 4. Experimental Results: (a) Test-I. (b) Test-II. (v_{gs}^B : 20 V/div), V_f : 3 V/div, i_{dc} : 100 A/div; X Scale: 400 ns/div.

IV. Experimental Results

The experimental setup of the 200 kW stack is shown in Fig. 3. +20/-5V is applied across the gate-source terminal of the device. $V_{dc(test)}$ =10 V is applied across the film capacitors. The ratings of the half-bridge SiC modules are tabulated in Table III. The details of the gate driver IC

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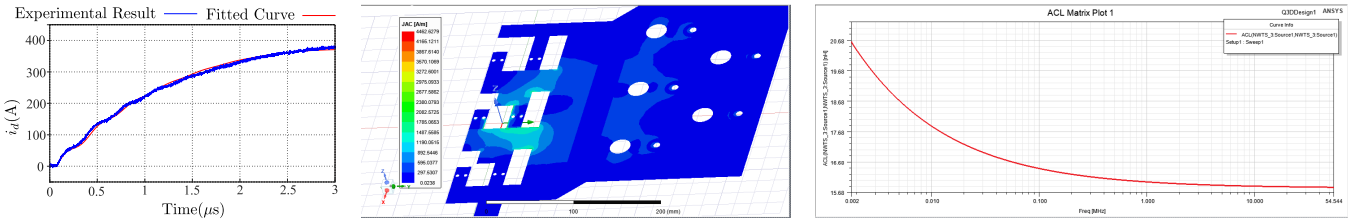

(a) (b) (c)

Fig. 5. (a) Experimental and fitted curve for Test-II. (b) Current density plot of DC bus-bar. (c) Simulation Result of DC bus-bar.

TABLE III
RATINGS OF SIC MODULE

Part Number	V_{ds}	I_{ds}	R_{on}	L_l
MSCSM120AM03CT6LIAG	1200 V	805 A	3.1 mΩ	3 nH

TABLE IV
DETAILS OF THE GATE DRIVER

Part Number	V_{in}	t_{pd}	V_{out}	I_{pk}
ADuM4135	2.5-6 V	40-70 ns	12-30 V	4 A

are given in Table IV. A 30 A (IXD630) current booster is placed after the gate driver to supply the required gate current during switching. Experimentally measured signals are gate-source voltage of Q_B (v_{gs}^B), V_f and i_d. Oscilloscope MDO3104 from Tektronix with 1GHz bandwidth is used. High voltage differential probe THDP0200 of 200GHz bandwidth and single-ended probe P5100A with 500 MHz bandwidth (both from Tektronix) are used for the measurement of V_f and v_{gs}^B, respectively. High current 50 MHz Rogowski sensor CWTMini50HF 06/B/1/100/2 from PEM is used to measure i_{dc}. The propagation delay between voltage and current signals is matched using a delay matching instrument from Tektronix (067-1686-00, Power Measurement De-skew and Calibration Fixture).

A. Test-I

Initially, the test is performed on the middle module, and the other two modules are removed. The experimental waveforms are shown in Fig. 4a. L_{eq} and R_{eq} is estimated from experimentally measured i_{dc} as discussed in Section 3 and the estimated values are 27 nH and 19.7 mΩ, respectively. Initially, 10 V is applied, and during measurement. The measured voltage across C_f drops to 8 V due to the inductive drop of its ESL, L_f (see Fig. 4a). The value of L_f can be estimated using (7). Please note estimated value is higher than the value obtained from the film capacitors' data-sheet.

$$\Delta v_{C_f} = L_f \frac{di_{dc}}{dt} \tag{7}$$

B. Test-II

Test-II is also performed on the middle module, keeping all other operating conditions similar to Test-I. The experimental result is presented in Fig. 4b. Given the total power loop inductance and L_f are known, the values of L_d, L_l, and L_{Tr}

TABLE V
EXPERIMENTAL AND SIMULATION RESULTS FOR MIDDLE MODULE

	Experimental	Simulation
L_f	8 nH	6 nH
L_d	13 nH	12 nH
L_{Tr}	8 nH	5 nH

TABLE VI
EXPERIMENTAL AND SIMULATION RESULTS FOR SIDE MODULE

	Experimental	Simulation
L_f	8 nH	6 nH
L_d	13 nH	13 nH
L_{Tr}	8 nH	5 nH

are estimated as discussed in Section III-B and tabulated in Table V. Here, L_l is coming around 7 nH. Fig. 5a represents the experimental results and fitted curve for Test-II, and they both match pretty closely.

Similarly, Test-I and Test-II are performed in any one of the side modules (as shown in Fig. 1c), keeping the other two modules disconnected and the results are tabulated in Table. VI. The value of L_l is estimated to be approximately 7 nH for the side modules also. It can be observed that the parasitic inductances, considering the middle and side modules, are almost the same.

V. SIMULATION RESULTS

To verify the correctness of the proposed parasitic measurement technique, electromagnetic simulation is performed on the DC bus-bar structure and transient capacitor board with the help of ANSYS Q3D Extractor. In the 3D model of the DC bus bar, the ESL of the film capacitors is also considered. The solution frequency of the simulation is kept at 1 GHz. Interpolating sweep is given from 1 kHz to 100 MHz, with a sample size of 500 and 0.5% tolerance band. The simulation results containing current stress on the DC bus and plot of parasitic inductance to frequency for the middle module are shown in Fig. 5b and 5c, respectively and tabulated in Table V. A similar simulation is performed on a transient capacitor board as well. It can be observed that the proposed parasitic measurement technique matches well with the values estimated using electromagnetic simulation. The simulation is performed for the side module as well, and the results are tabulated in Table VI. The simulation and the experimental results

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match well. This validates the correctness of the proposed measurement technique.

VI. Conclusion

This paper proposes an experimental approach to extract the parasitics involved in switching transition for a 200 kW SiC-based stack. To verify the proposed methodology, an electromagnetic simulation is performed on the 3D models of the DC bus-bar and transient capacitor board for extracting the parasitics through simulation with the help of ANSYS Q3D Extractor. Finally, the parasitic inductances extracted by the proposed method and simulation are compared and found to match well, which verifies the efficacy of the proposed method.

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