2023 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE) | 979-8-3503-1057-3/23/$31.00 ©2023 IEEE | DOI: 10.1109/PESGRE58662.2023.10404507

Layout Design of a 1.2kV 5kW 50kHz SiC-based Neutral-Point-Clamped leg for a Modular Medium Voltage AC to LVDC Solid-State-Transformer

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***Abstract*—Medium voltage AC (MVAC) to low voltage DC (LVDC) solid-state transformers are an emerging area of power electronics. This application requires bidirectional MVAC to LVDC converters with high efficiency and power density. The use of wide band gap SiC-based devices has increased the operating frequency of solid-state transformers leading to reduced size and higher efficiency. Modular solutions using low-voltage devices are widely adopted, and the number of modules involved in such converters is directly related to the MVAC level and device voltage rating. Module count and, thus, the device count can be reduced by adopting a multi-level architecture with the module to increase the module voltage rating.**

In this paper, the design and development of a 1.2kV SiC-based three-level, three-phase NPC leg is presented, which is the building block of the MVAC-LVDC converter. The layout design of a NPC leg is challenging due to the existence of multiple commutation loops (4) involving more number of devices. Challenges associated with designing the Neutral point clamped (NPC) leg and minimizing the loop inductance in the commutation loops are addressed, enabling switching at 50kHz while processing 5kW power. A novel four-layer layout is proposed with individual high frequency decoupling capacitance with damping resistance for four commutation loops. The bigger commutation loop with four devices is optimized with a trade-off in the smaller loop to minimize the worst-case switching transient. Experimental results for the module at rated conditions are also presented in the paper for the DAB stage with power density higher than 1.5kW/L and peak efficiency of 97%.

***Index Terms*—Stability analysis, Continuous control set model predictive control, CCS-MPC, dead beat control, Buck converter.**

I. Introduction

Modular MVAC to LVDC converter with high-frequency link isolation is an emerging solution for a wide range of applications, including electric vehicle fast charging, grid integration of renewable, high capacity grid-connected storage system, hydrogen production, etc. [1]–[3]. The modules are realized with commercially available low voltage devices due to their robustness [2], [4], [5]. The module count in these solutions is a ratio of the voltage level at the AC side to the module voltage rating. The module count and, further, the device count can be reduced by having a higher voltage module, which can be realized with multilevel architecture.

Neutral point clamped (NPC) leg is one of the popular multi level architecture existing in literature for wide range of applications [6], [7]. Design of NPC leg is challenging due to the involvement of multiple commutation loops with more number of devices, unlike H-bridge. H bridge made of four devices have two commutation loops involving two devices, this can be achieved by placing both devices nearby to limit the loop inductance. For NPC there are six devices in total and there are four commutation loop involving two or four devices [8] which makes the design challenging.

An MVAC to LVDC converter is proposed in [9] which utilities multi level architecture within the module as shown in Fig. 1. A single phase module for this topology is also shown in detail. The design and development of the NPC leg within a single-phase module are presented in this paper for an 11kV 120kW prototype. Specification and converter operation is discussed in the second section. NPC leg design is given in the third section, and the experimental results are provided in section IV. The fifth section concludes the paper.

II. Single-phase module

The highlighted single-phase module is a combination of an unfolder (line frequency switched H-bridge), NPC leg (high frequency switched), the high-frequency transformer (HFT), inductor, and an H-bridge (high frequency switched) at the DC side. The module voltage rating depends on the DC bus voltage of the unfolder and NPC leg. The unfolder is realized with a higher voltage-rated conduction loss-optimized device as it switches at the zero crossing of the line cycle.

Design of a single-phase module is carried out for a 120kW, 11kV MVAC to 800V LVDC prototype with a switching frequency of 50 kHz. The DC bus voltage of the NPC leg is 1200V, and the device in the NPC leg sees a voltage of half the DC bus voltage, which is 600V. The peak phase voltage for 11kV MVAC grid is 9kV ($11 * \sqrt{2}/\sqrt{3} = 8.98$),

This work was supported in part by the Department of Science and Technology, Government of India, under the project titled "Medium Voltage Grid Integration of Utility-Scale Renewable " through the Core Research Grant scheme.

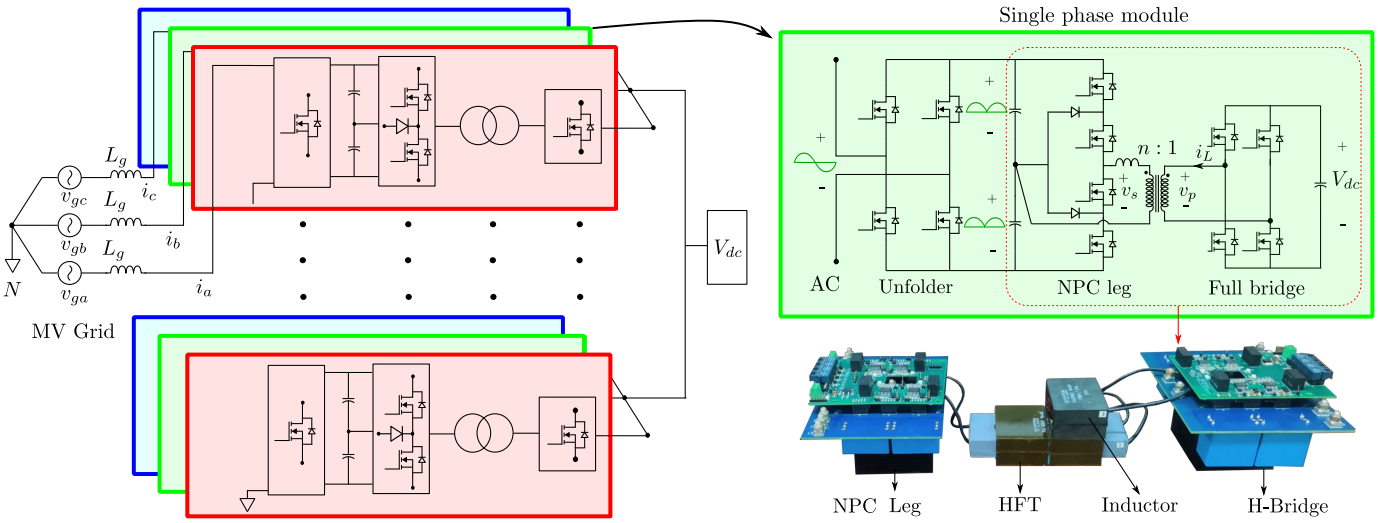


Fig. 1: Modular MVAC to LVDC converter with multi level architecture within the module

and the number of modules required to reach 11kV is 8 $(8.98/1.2 = 7.48)$. The power rating of a single-phase module for a 120kW prototype is 5kW $(120/(3 * 8))$. 1200V SiC MOSFETs are selected for both the high-frequency switched bridges, including the NPC leg and H bridge at the DC side. 1700V SiC MOSFETs with lower on-resistance are used in the unfolder, and these devices block the DC bus voltage of 1200V. Therefore, the peak phase voltage of a single-phase module is 1.2kV.

III. Design of the Converter

A. Layout optimization

The design of the NPC leg is critical as it has more commutation loops per leg and sees higher DC bus voltage compared to the device rating. 1200V SiC MOSFETs from Genesic, G3R30MT12K and 1200V SiC diode from CREE, C4D20120H are used in the NPC leg. One leg is made using four MOSFETs and two diodes, as seen in Fig. 2. These six devices need to be arranged in a power board with minimal parasitic inductance in the four commutation loops involved. Heat sink OMNI-UNI-41-L from Wakefield-vette is selected based on thermal design to mount six devices of the NPC within a board while maintaining the junction temperature below safe limits.

A symmetric arrangement is followed with two MOSFETs and one diode on each side of the heat sink. Two commutation loops involved during the switching transient (given in Fig. 2) are symmetric to the other two, and therefore, it is sufficient

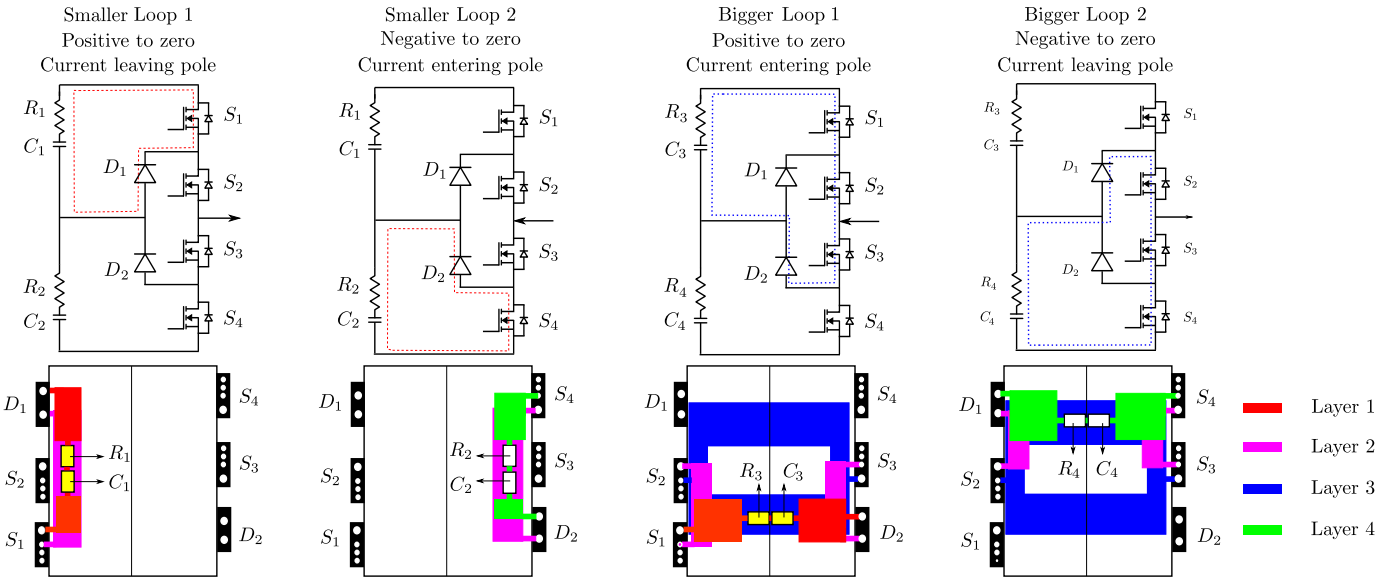


Fig. 2: Four layer Layout plan for NPC leg considering four commutation loops involved during different switching transients. The commutation loop inductance is optimized by sandwiching paths that carry current in opposite direction in each loop.

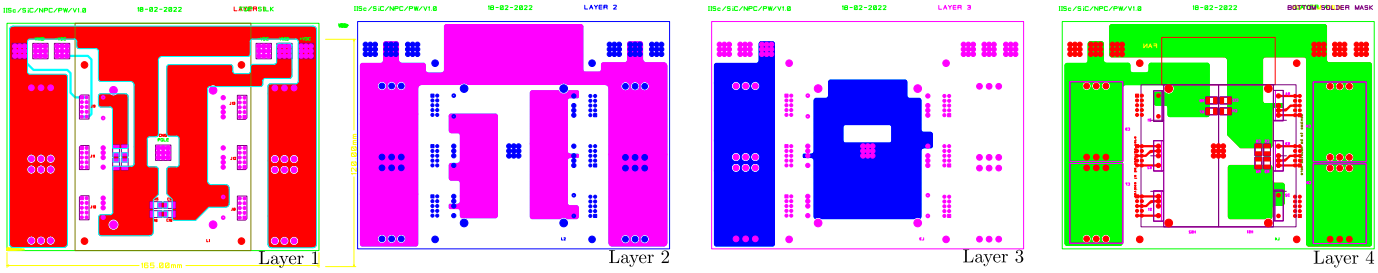


Fig. 3: Four layer Layout for NPC leg power PCB with minimized parasitic inductance.

to consider only two loops. During the transition between the positive and zero states with current leaving the pole, current flows through S_1 and S_2 during the positive state and through D_1 and S_2 during the zero state. Therefore the current transition happens in S_1 and D_1, forming the smaller commutation loop 1 involving only two devices. Similarly, the other smaller commutation loop 2 is formed by S_4 and D_2 when the NPC leg transit between negative and zero states with current entering the pole. The top larger commutation loop 3 is active for the transition between positive and zero states with the current entering the pole. During the positive state, the current flows through S_1 and S_2, and during the zero state, it flows through S_3 and D_2 for a larger loop involving S_1, S_2, S_3 and D_2. Similarly, the larger commutation loop 4 is formed during the transition between zero and negative state with the current leaving the pole involving S_2, S_3, S_4, and D_1.

The larger loop and its parasitic inductance are prioritized as these loops contribute to high voltage oscillation during the switching transient. The six devices are arranged on both sides of the heat sink within a four-layer PCB with maximum possible sandwiching between layers involved conduction loops as shown in Fig. 2. Tracks in different layers are shown in different colours. This layout is fabricated as shown in Fig. 4 (NPC leg power board), and a double pulse test is conducted to verify the switching transient waveform. A double pulse test is conducted by connecting an inductor between two terminals in four configurations, as shown in Fig. 5 - 8. Turn on and turn off transient for loop1 (smaller loop), loop2 (smaller loop), loop 3 (bigger loop) and loop 4 (bigger loop) are given in these figures. As expected, the switching transient involving the bigger loop exhibited higher oscillation in drain-source voltage during turn-off. The experiment is conducted with half DC bus voltage up to 800V and drain current up to 30A. It is observed the overshoot and oscillation in drain-source voltage and dv/dt is restricted within safe limits.

B. Gate driver design

The gate driver board is designed with the gate driver IC ADuM4135 from Analog devices. It has four drivers and can drive four independent switches. The PWM signals are received through optical receivers (HFBR-2532ETZ) as shown in Fig. 4. isolated power supply from Murata MGJ2D151505SC is used to power the gate driver IC from auxiliary power. The board is compatible with the NPC leg power board to form a modular assembly, as shown.

IV. Results

The specification of the multilevel Dual active bridge (DAB) made with a combination of H-bridge and NPC leg are given in Table. I and the hardware picture is shown in Fig. 1. The schematic for this is also given in Fig. 1, which is going to be there in the single-phase module for the solid-state transformer. A double pulse test is conducted for the converter at a current of 30A with the configurations shown in Fig. 5 - 8. There are four commutation loops in the NPC leg; two are symmetric with respect to the other. Four double pulse results are given for different configurations, two for bigger loops and the other two for a smaller loops. The switching transient waveform are also shown in these figures. The DAB is operated at a 5kW power level; voltage and current waveform are given in Fig.

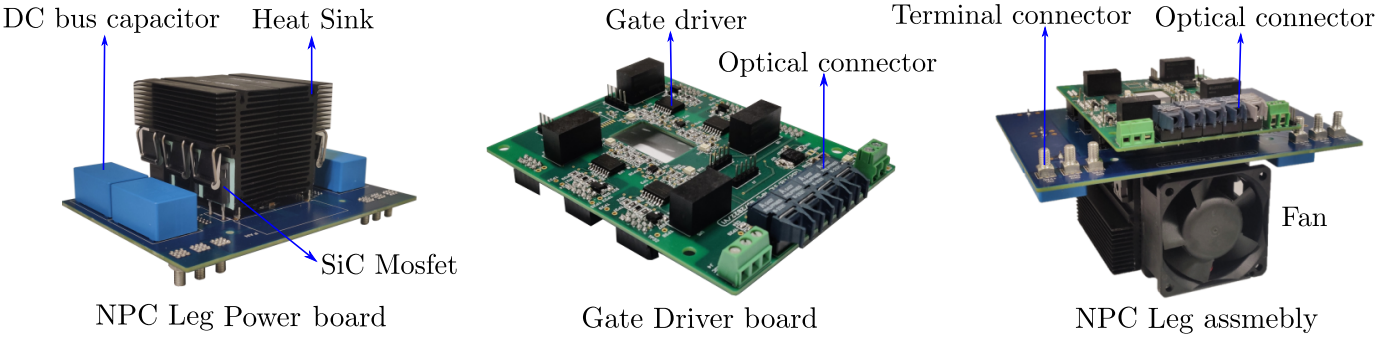
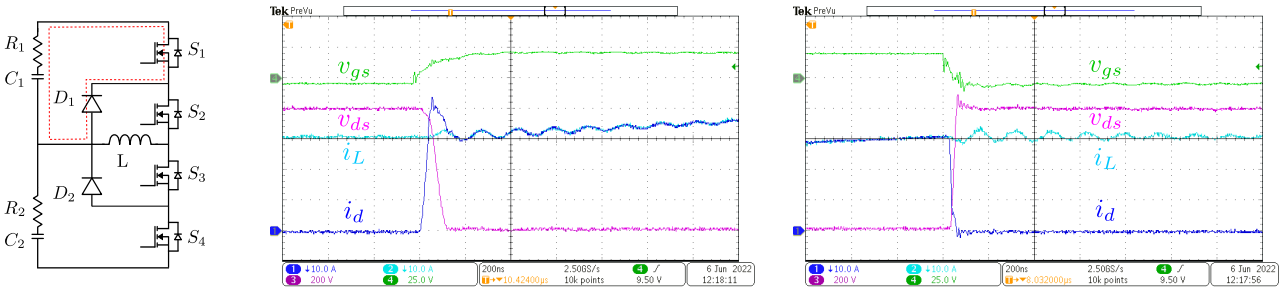
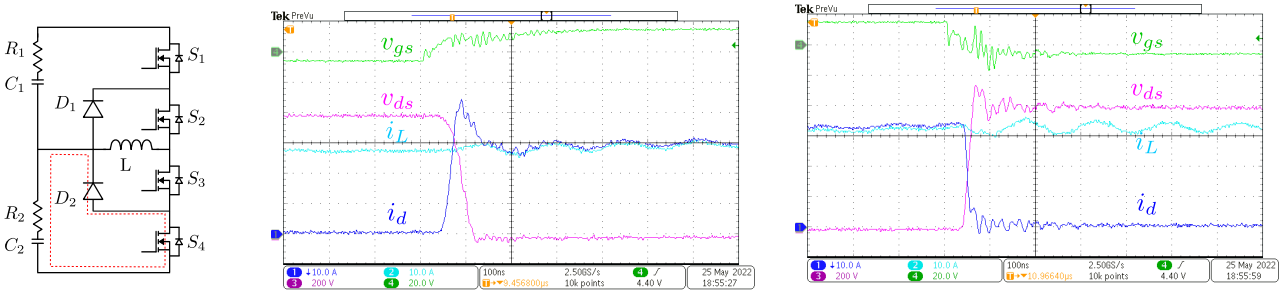


Fig. 4: Modular SiC power board and gate driver board for the NPC leg assembly.



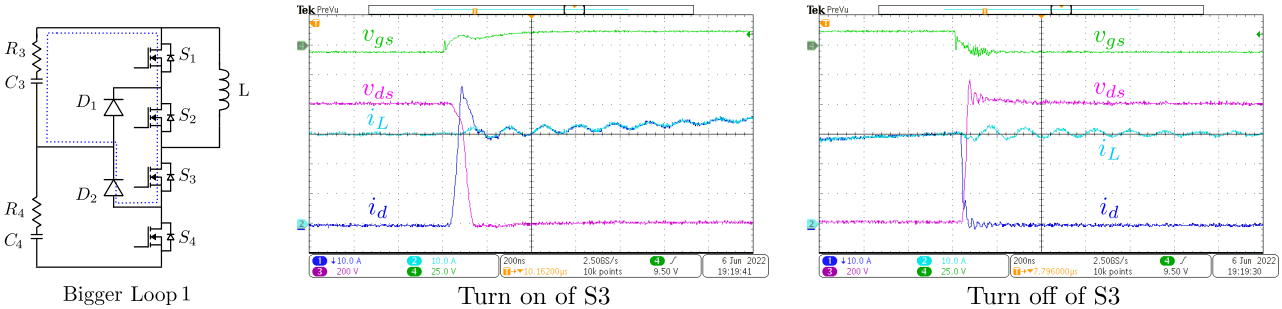
Smaller Loop 1 Turn on of S1 Turn off of S1

Fig. 5: Double pulse test schematic and transition results for smaller loop 1 at 30A. The turn on transition happens when the MOSFET S1 is turned on from the state when current was freewheeling through $L, -D_1, -S_2$ and after the transition current flows through DC bus (R_1C_1) $-S_1 - S_2 - L$. Reverse for turn off transition.



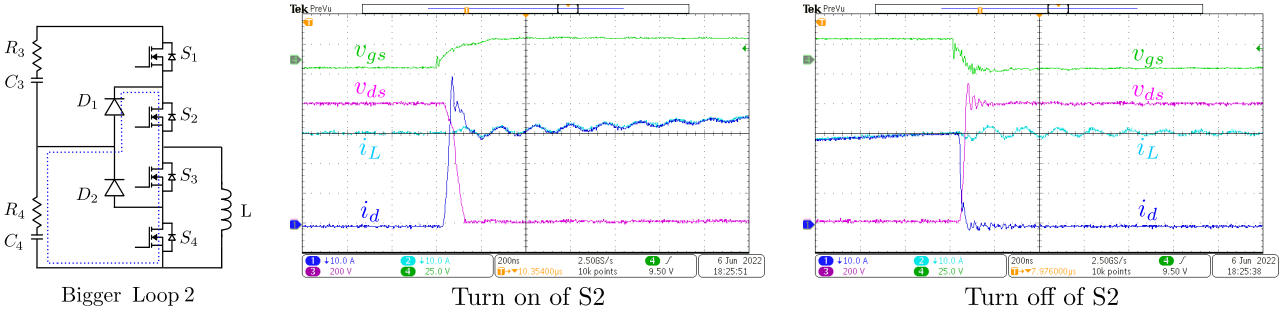
Smaller Loop 2 Turn on of S4 Turn off of S4

Fig. 6: Double pulse test schematic and transition results for smaller loop 2 at 30A. The turn on transition happens when the MOSFET S4 is turned on from the state when current was freewheeling through $L, -D_2, -S_3$ and after the transition current flows through DC bus (R_2C_2) $-L - S_3 - S_4$. Reverse for turn off transition.



Bigger Loop 1 Turn on of S3 Turn off of S3

Fig. 7: Double pulse test schematic and transition results for bigger loop 1 at 30A. The turn on transition happens when the MOSFET S3 is turned on from the state when current was freewheeling through $L, -S_1, -S_2$ and after the transition current flows through DC bus (R_1C_1) $-L - S_3 - D_2$. Reverse for turn off transition.



Bigger Loop 2 Turn on of S2 Turn off of S2

Fig. 8: Double pulse test schematic and transition results for bigger loop 2 at 30A. The turn on transition happens when the MOSFET S2 is turned on from the state when current was freewheeling through $L, -S_3, -S_4$ and after the transition current flows through DC bus (R_2C_2) $-D_1 - S_2 - L$. Reverse for turn off transition.

Parameter	Symbol	Value
NPC DC Voltage	(V_{dc}^{npc})	1200 V
DC bus Voltage	(V_{dc})	800 V
Module power rating	(P_o)	5 kW
Switching frequency	(f_s)	50 kHz
Transformer turns ratio	(n)	0.8
Series inductance	(L)	$140\mu H$
Power density	(Pd)	1.5kW/L
Peak efficiency	(η)	97%

TABLE I: Specification of the developed multilevel DAB stage for a single-phase module

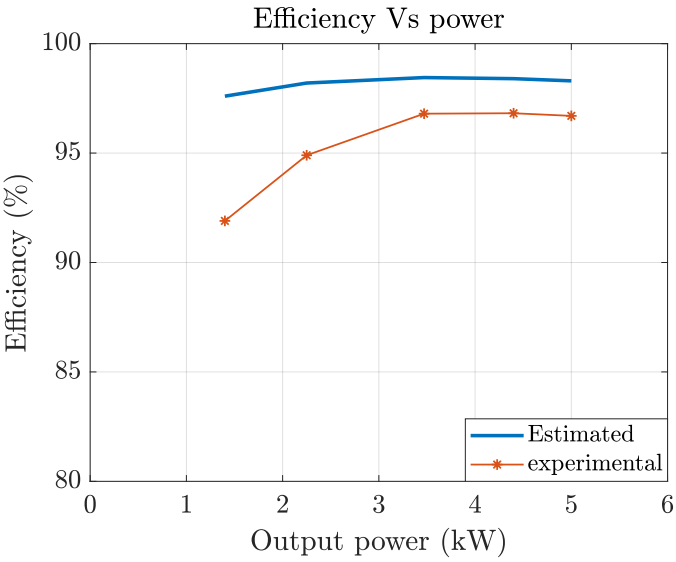


Fig. 9: High frequency voltage and current waveform at 5kW rated power and 1200V at NPC DC bus

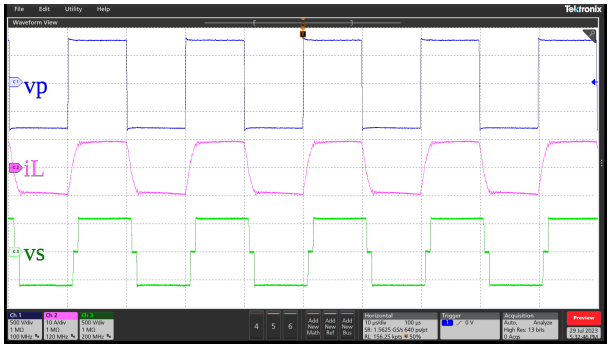


Fig. 10: High frequency voltage and current waveform at 5kW rated power and 1200V at NPC DC bus, Ch1: Primary voltage (v_p), Ch2: Inductor current (i_L), Ch3: Secondary voltage (v_s), refer Fig. 1.

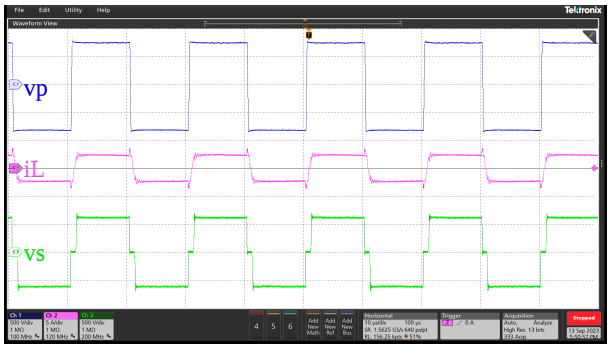


Fig. 11: High frequency voltage and current waveform at 1kW rated power and 1200V at NPC DC bus, Ch1: Primary voltage (v_p), Ch2: Inductor current (i_L), Ch3: Secondary voltage (v_s), refer Fig. 1.

10. The peak efficiency of the module is 97% at 3.5kW output power.

V. Conclusion

In conclusion, the design of a 1.2kV, 5kW SiC-based three-level NPC leg for a DAB converter with a switching frequency of 50kHz has been presented in this paper. The paper addresses the challenges associated with designing the NPC leg and minimizing the loop inductance in the commutation loops, contributing to the development of more efficient and compact SST modules. The experimental results demonstrate the switching transient waveform is within safe limits and high-frequency waveform in DAB operation is as expected. Furthermore, the study highlights the benefits of SiC devices in solid-state transformer applications, leading to reduced filter sizes and more compact and efficient converters. A prototype with a power density greater than 1.5kW/L and a peak efficiency of 97% is designed and developed. Overall, the paper provides a valuable methodology for designing high-power SiC-based modules for solid-state transformers.

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