Design and Development of Three-Phase High-Frequency AC Power Distribution Architecture for Space Application

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***Abstract*— This paper proposes a new three-phase (3ϕ) high-frequency ac (HFAC) power distribution architecture for space applications. Advantages of this approach include high-quality HFAC generation with improved THD, load-independent voltage gain, etc. A design procedure for a 10kHz ac power distribution is detailed. Inverter switching frequency is selected around 200 kHz. A systematic method is adopted for selecting the inverter switches based on specific performance parameters and power loss. Considering sine-triangle PWM, the AC-side filter inductor is designed to keep the inductor current ripple within a specified limit. The filter capacitor is also selected based on a ripple criterion. Since the inverter is switched at 200 kHz, the critical considerations for high-frequency PCB layout are also discussed. Finally, the proposed inverter design approach is validated experimentally at 1kW, 30 $V_{ph(peak)}$, 10 kHz 3ϕ HFAC system.**

***Index Terms*—High-frequency PWM inveter, trap filters, LC filter.**

I. Introduction

Conventional DC power distribution for satellites supported by PV panels employ an isolated DC-DC converter to step down the voltage, followed by a point-of-load (PoL) converter at each load end (Fig. 1a) [1]. Due to a large number of radar loads, a large number of isolated DC-DC converters are used. Multiple isolated DC-DC converters increase the system's cost, complexity and productisation challenges. An alternative solution can be high-frequency AC (HFAC) power distribution architecture (Fig. 1b). At the load end, a high-frequency transformer (HFT) can step down, and then a simple diode bridge is used to rectify the voltage before feeding it to the PoL. This approach mitigates any gate driver requirement and control logic for each load end. The AC must be high frequency to keep the transformer size small.

The HFAC power distribution architecture for satellites was first implemented by NASA [1]. Due to the lack of fast switching devices, classical DC-HFAC systems employed parallel resonant inverters [2]- [3]. The load-dependent gain property of the parallel resonant converter makes this approach quite complex for paralleling and control. A pre-regulator buck stage can address some of these issues at the cost of reduced efficiency due to multiple power conversion stages.

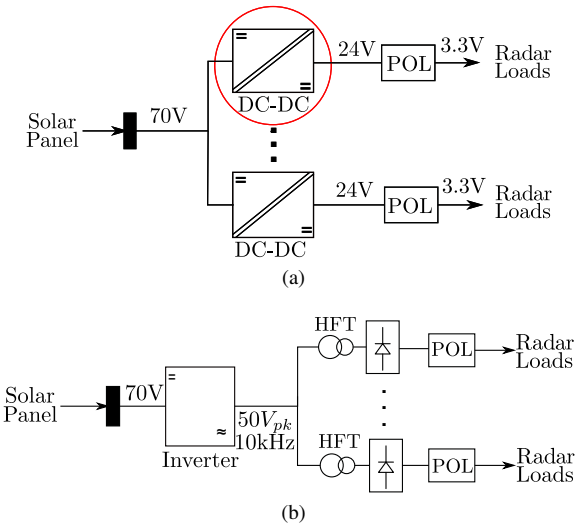


Fig. 1. Conventional power distribution for Satellites (a) DC architecture, (b) 1-phase HFAC architecture.

On the other hand, the inherent load-independent nature and seamless parallel operation make the PWM inverter a suitable choice for HFAC application. The PWM inverters need the switching frequency to be 20 times higher than the fundamental frequency, which can be achieved using current power semiconductor devices.

In [7], the PWM-based HFAC power architecture for satellite application is discussed where power transistors were employed to generate high frequency (13 kHz) quasi trapezoidal voltage to cater for the low-voltage transformer-rectifier type power supplies as well as high voltage power supplies. But in the case of radar load application, the quasi-trapezoidal current can cause a significant harmonic drop in the inductive power line. So, the high-quality, high-frequency voltage must be produced to distribute the power.

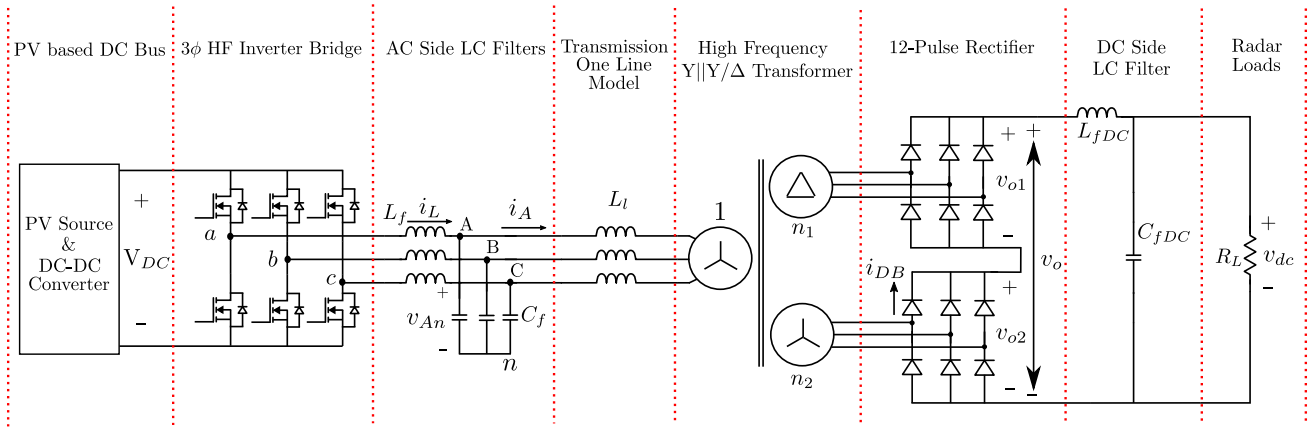


Fig. 2. Proposed Three-phase (3-ϕ) 10 kHz HFAC Power Distribution Architecture for Satellites

The design of a single-phase (1ϕ) PWM-based HFAC system (Fig. 1b) is proposed, and its control is described in [5], [6], respectively. Since the 1ϕ diode bridge rectifier draws square wave current, trap filters (at least up to 9^{th} harmonic) are placed before it to restrict the harmonic currents flowing through the inductive power line [6]. The component tolerances make tuning the traps at the desired frequencies difficult, leading to poor THD in the line current (around 16.94%) [5]. Also, the inclusion of traps makes the control of this system quite complicated and challenging [6].

These limitations of the 1ϕ PWM inverter-based HFAC system are addressed in this paper by introducing a 3ϕ power architecture. The advantages of the proposed topology include (a) high-frequency (10 kHz) power distribution with improved THD, (b) LC filter with high-frequency transformer ($Y||Y/\Delta$) is sufficient enough to filter out the harmonics. (c) Trap filters are not required, which improves reliability. (d) Load independent voltage gain.

The main contributions of this paper are as follows. 1) The working principle of the proposed 3ϕ HFAC system is detailed. 2) A systematic procedure is presented for switch selection. 3) The steps associated with the filter inductor design are highlighted. 4) A simplified approach is presented for designing the filter capacitor. 5) The critical considerations for component placement and PCB layout are described adequately.

The organization of the paper is as follows: Section II presents the whole power train of the proposed 3ϕ HFAC architecture. The design steps are detailed in Section III. The details of hardware development are given in Section IV. The experimental results are presented in Section V. Finally, the paper is concluded in Section VI.

II. Proposed System Architecture

The complete power train of the proposed 3ϕ HFAC distribution scheme is shown in Fig. 2. The Si-MOSFET-based HFAC inverter bridge is indicated. The input of the bridge is connected to a DC bus V_{DC}. The output of the HFAC inverter bridge is filtered using a low pass LC filter (L_f and C_f), and the filter output is connected to the star-connected primary of the high-frequency transformer (HFT) through the power line. L_l represents the lumped inductance model of the long power line cable along with the primary side leakage inductance of the transformer. In the secondary, star and delta windings are connected to the input of two separate 3ϕ rectifiers, and the outputs are connected in series to form the twelve-pulse rectified output. As the first harmonic component of the current drawn by the twelve-pulse rectifier is of 11^{th} order, trap filters can be eliminated, which makes this system more efficient and reliable and reduces the control challenges. The output of the twelve-pulse rectifier is filtered using the DC side filter L_{fDC} and C_{fDC}, respectively. R_L represents the concentrated resistive load. In actual practice, each load end will have a configuration shown in Fig. 2 and be connected in parallel. The overall system specifications are listed in Table I. Sine-triangle modulation technique is adopted for the high-frequency inverter. Modulation index M is defined as $(V_{An_{pk}}/V_{DC})$. Thus, the duty ratio of a, b and c phases are $d_a = (1/2) + M\sin\theta$, $d_b = (1/2) + M\sin(\theta - (2\pi/3))$ and $d_c = (1/2) + M\sin(\theta + (2\pi/3))$, respectively where $\theta = 2\pi f_o t$. Note that the size of the transformer will remain similar to that of the single-phase solution since each secondary handles half of the total power rating (P_o) of the system.

TABLE I
Specification of 3ϕ HFAC System

V_{DC}	$V_{An_{pk}}$	P_o	f_o	f_s	L_l	$1 : n_1 : n_2$
80V	30V	1kW	10kHz	200kHz	3.3μH	$1 : \sqrt{(3)} : 1$

III. Design Steps of High Frequency Inverter

This section describes the design and selection procedures of different components of the 3ϕ high-frequency AC inverter.

A. Switch and Gate Driver Selection

Based on the availability of the space-grade variants, Si MOSFETs from different manufacturers are evaluated for this design. The devices considered have 150V blocking

TABLE II
DETAILS OF THE GATE DRIVER.

Part Number	V_{in}	t_{pd}	V_{out}	I_{pk}
1EDB827	3-15V	45ns	Upto 20V	5 A

voltage and a current rating ranging from 50A to 130A. Since the 3ϕ inverter is hard-switched, diode reverse recovery loss substantially contributes to the total switching loss at high switching frequencies. So, the Si MOSFETs with low body diode reverse recovery charge (Q_{rr}) and time (t_{rr}) are considered. Total switching loss and corresponding junction temperature are obtained for each selected device. However, the procedure is explained below considering the chosen device, IPP051N15N5AKSA1 (150V, 120A) from Infineon.

LTSpice simulation is carried out to obtain the switching loss as a function of current. The circuit configuration is given in Fig. 3a. The input DC voltage is V_{dc}=80V, and the filter inductor current (I_L) is varied in the range (5, 40)A in steps of 5A. v_{gs} is applied around -2V/+10V, and 10 Ω and 4.5 Ω are the gate-resistances for the ON and OFF transitions, respectively. A lumped parasitic power loop inductance (L_{dc}) of 10 nH is considered for the initial simulation. The total switching loss (E_{SW}) is extracted from the simulation and plotted as a function of I_L in Fig. 3b.

After obtaining E_{SW} vs I_L plot, a second order polynomial is fitted ($E_{SW} = a * i^2 + b * i + c$) and the extracted parameters are $a = 0.04373\ \mu J/A^2$, $b = 2.227\ \mu J/A$ and $c = 20.55\ \mu J$ (see Fig. 3b). Neglecting the inductor current ripple, the total switching power loss (P_{SW}) is obtained using (1) where $i = I_{PK} \sin\theta$. I_{PK} represents the peak value of the fundamental inductor current. Similarly, the conduction loss (P_C) is obtained using (2) where $R_{on} = 5.75m\Omega$ is the on-state resistance of the selected Si MOSFET @100^oC. The total loss $P = (P_c + P_{SW}) = 6.26\ W$. For the selected device, junction-to-case thermal resistance (R_{jc}) is $0.3^oC/W$. Thermal interface material PL-05-5-1016-H from Wakefield-Vette is used, and the case to heatsink thermal resistance (R_{ch}) is estimated to be $0.98^oC/W$.

Assuming the heatsink temperature is maintained at $T_{hs} = 60^o$ C, junction temperature T_j can be estimated as 68.01^o C using (3) and it is less than 175^o C (maximum allowable junction temperature).

$$P_{SW} = \frac{1}{2\pi}\int_0^{\pi} E_{SW}\ d\theta \tag{1}$$

$$P_C = \frac{I_{PK}^2 R_{on}}{4} \tag{2}$$

$$T_j = T_{hs} + (R_{jc} + R_{ch}) \times P \tag{3}$$

The details of the selected gate driver are given in Table II.

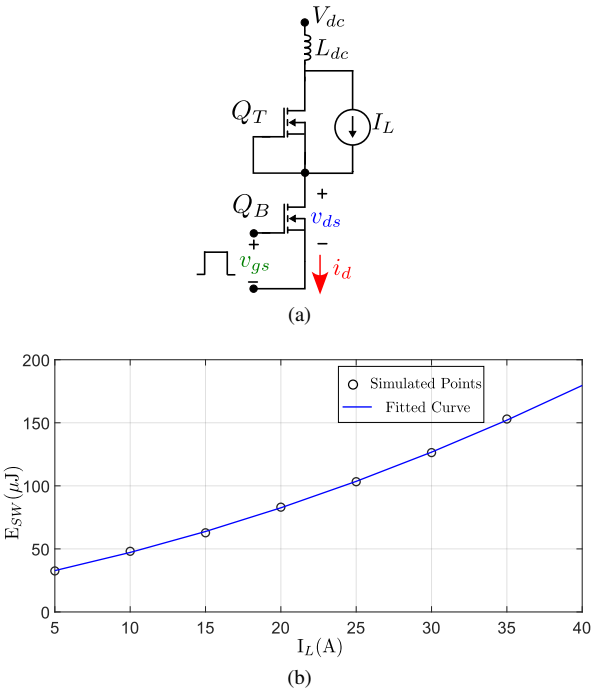


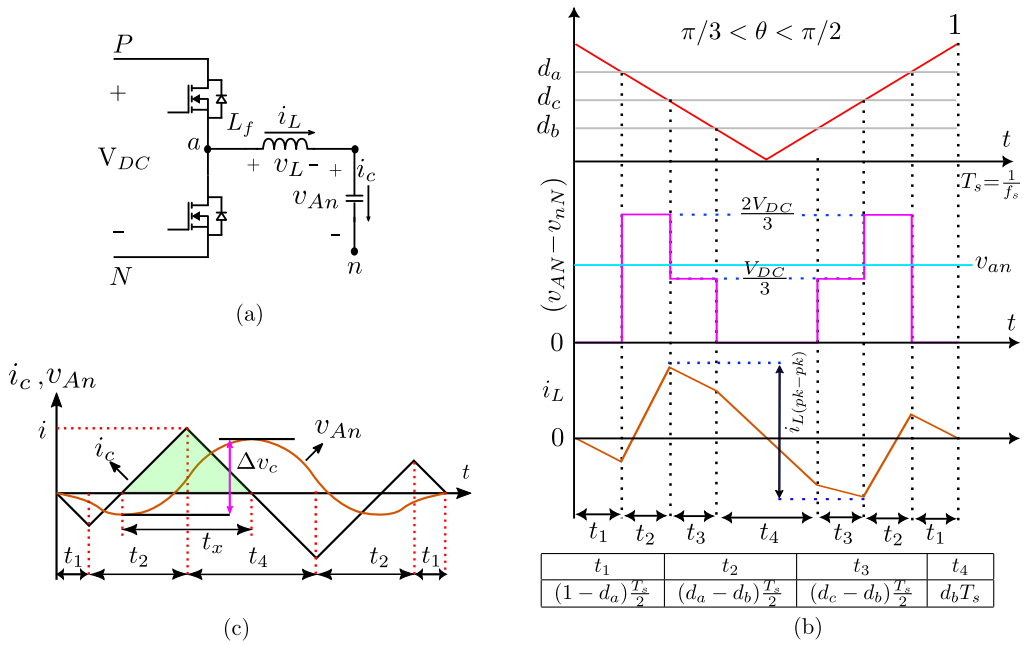
Fig. 3. (a) Double-pulse test circuit. (b) Variation in E_{sw} with varying I_L.

B. AC Filter Inductor (L_f) Design

In literature, the filter inductor design approaches are available for 50 Hz inverters considering space vector and bus-clamp PWM techniques [7], [8]. Note digital controllers are avoided for this application. Because of easy analog implementation, SPWM is adopted in this work. The associated L_f design is carried out as follows. The value of L_f is selected from the maximum peak to peak ripple ($i_{L(pk-pk)(max)}$) consideration of the inductor current i_L. To express $i_{L(pk-pk)}$ as a function of V_{DC}, L_f, M and θ, it is assumed that the voltage across C_f is sinusoidal and ripple-free and it remains approximately constant over a switching period.

However, analysing a quarter cycle is sufficient due to the quasi-square-wave symmetry in i_L. This corresponds to two different sectors, which are $-\pi/6 \le \theta \le \pi/6$ and $\pi/6 \le \theta \le \pi/2$.

An equivalent circuit of phase-a is shown in Fig. 4(a). The voltage across L_f ($v_L = v_{AN} - v_{an} - v_{nN}$) is integrated over the applied time duration to estimate peak-to-peak ripple current ($i_{L(pk-pk)}$). Table III contains the $i_{L(pk-pk)}$ expressions of the sectors as mentioned above. Please note, for the sector $\pi/6 \le \theta \le \pi/2$, there can be two different expressions for $i_{L(pk-pk)}$ based on whether (i) $v_{an} < (V_{DC}/3)$, and (ii) $v_{an} > (V_{DC}/3)$. In Fig. 4(b), the sample waveforms of the $(v_{AN} - v_{nN})$ and i_L are shown for the sector of $\pi/6 \le \theta \le \pi/2$, and $v_{an} > V_{DC}/3$. The expression corresponding to maximum ripple is given in (4), which needs to be considered while designing the L_f.



t_1	t_2	t_3	t_4
$(1-d_a)\frac{T_s}{2}$	$(d_a-d_b)\frac{T_s}{2}$	$(d_c-d_b)\frac{T_s}{2}$	d_bT_s

Fig. 4. (a) Equivalent circuit of phase-a of proposed HFAC shown in Fig.2. (b) Waveforms during one switching period. (c) Waveform of capacitor current (i_c) and voltage (v_{An}) of phase-a.

TABLE III
EXPRESSIONS OF $i_{L(pk-pk)}$

$0<\theta<(\pi/6)$	$(\pi/6)<\theta<(\pi/2)$	
	$v_{an}<\frac{V_{DC}}{3}$	$v_{an}>\frac{V_{DC}}{3}$
$i_{L(pk-pk)1}=-\left(\frac{v_{an}}{L}\right)T_s max\{d_b,(1-d_a)\}$	$i_{L(pk-pk)2}=-\left(\frac{v_{an}}{L}\right)T_s max\{d_b,(1-d_a)\}$	$i_{L(pk-pk)3}=max\left\{\frac{\left(\frac{V_{DC}}{3}-v_{an}\right)}{L}(d_c-d_b)T_s-\frac{v_{an}}{L}d_cT_s,-\left(\frac{v_{an}}{L}\right)(1-d_a)T_s\right\}$

$$i_{L(pk-pk)(max)}=max(i_{L(pk-pk)1},i_{L(pk-pk)2},i_{L(pk-pk)3}) \quad (4)$$

For the designed converter, the maximum peak-peak ripple occurs at $\theta=\pi/2$. As, V_{DC}=80 V, $v_{an(pk)}$=30V $\geq (V_{DC}/3)$, the expression of $i_{L(pk-pk)3}$ in Table III is considered for designing L_f. The $i_{L(pk-pk)}$ is considered 30% of the fundamental peak current results in L_f=7μH.

C. AC Filter capacitor (C_f) Design

The entire inductor ripple current (Δi_L) is assumed to flow through the capacitor. So, the voltage ripple will be maximum wherever the area under the curve of i_c (highlighted in green in Fig. 4(c) will be maximum. Now, at $\theta=\pi/2$, $d_c=d_b$ so the ripple in the inductor current (shown in Fig. 4(b)) will be modified as shown in Fig. 4(c) (waveform of i_c). Now, the C_f can be calculated as $C_f=\frac{\Delta Q}{\Delta v_{An}}$, where ΔQ is the area under the curve highlighted in green in i_c in Fig. 4(c) and can be represented as $\Delta Q=\frac{1}{2}it_x$, and the expression of C_f is given in (5).

$$C_f=\frac{MV_{DC}T_s^2\left(M-1\right)^2}{\left(32-48M\right)L_fv_{c(pk-pk)}} \quad (5)$$

IV. HARDWARE SET UP

The details of the hardware setup of the high-frequency inverter are given in this section. Fig. 5a and Fig. 5b describe the high-frequency inverter's overall floor plan and hardware picture, respectively. Selected Si MOSFETs are of TO-220 package and are vertically attached to the heat sink. Film and electrolytic capacitors are placed at the input DC bus to supply switching frequency and maintain constant dc bus voltage during load transients. Also, transient ceramic capacitors are placed close to the device to minimize the power loop inductance, reducing voltage overshoot.

Each half bridge contains both $V_{DC}+(P)$ and $V_{DC}-(N)$ and mid point connections [Refer Fig. 2]. Due to layout, the parasitic capacitance will form between $V_{DC}+(P)$ and $V_{DC}-(N)$ planes with respect to the midpoint. The overlap between the midpoint and $V_{DC}+(P)$ and $V_{DC}-(N)$ planes are minimized to minimize these parasitic capacitances. This helps to optimize the dead time between the complementary devices in a half-bridge. Also, separate gate driver cards are placed close to the device to drive the Si MOSFETs. Ferrite core along with Litz wire is used to design L_f. Film capacitors are used as C_f. The picture of the load board is given in Fig. 5c. This contains six single-phase transformers in star delta configurations respectively. The output is connected to the LC filter through a diode bridge (APT30S20BCTG).

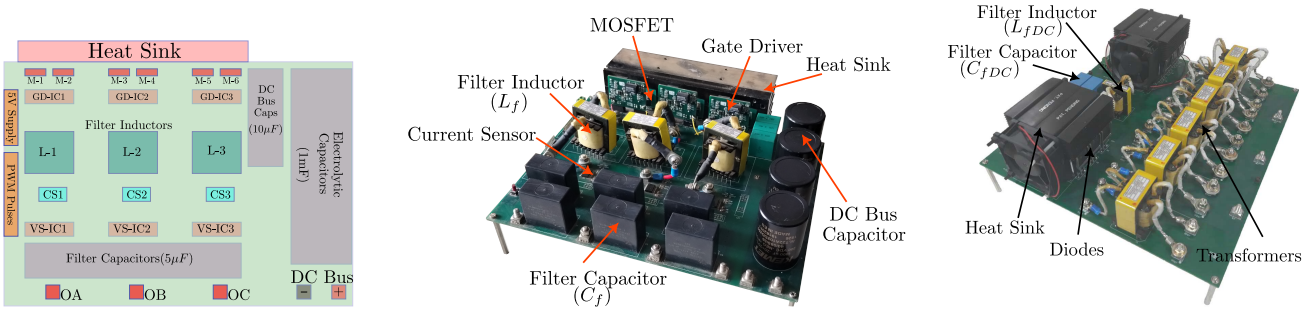


Fig. 5. (a) Power Board Layout. (b) Power Board Prototype. (c) Load Board.

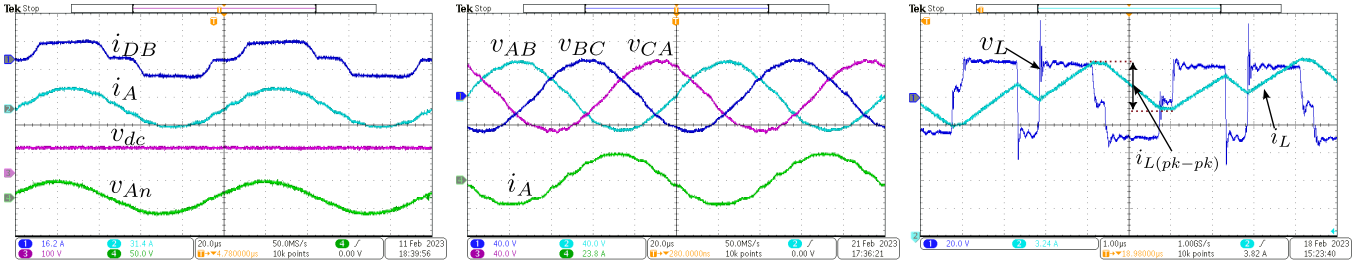


Fig. 6. Experimental Results: (a) Diode bridge current, i_{DB}(16.2A/div); Line current of phase-a, i_A(31.4A/div); Output voltage, v_{dc}(100V/div); Voltage of phase-a, v_{An}(50V/div); Scale: 20μs/div. (b) Line voltages of three phases, v_{ab}, v_{bc}, v_{ca} (40V/div); Line current of phase-a, i_A 23.8(A/div); Scale: 20μs/div. (c) Voltage and current of AC side filter inductor and v_L(50V/div), i_L(24A/div); Scale: 1μs/div.

V. Results and Discussions

The experimental results of 1 kW, 80V DC, 30 $V_{ph(pk)}$, 10 kHz 3ϕ HFAC inverter feeding non-linear load are presented in Fig. 6. In Fig. 6a, the input current (i_{DB}) of the diode bridge is shown along with the inverter output phase voltage (v_{An}) and current (i_A), and DC output voltage (v_{dc}) [Refer. Fig. 2]. As the 3ϕ diode bridge rectifier draws a quasi-square wave current (i_{DB}), it will not have triplen harmonics. Furthermore, with the introduction of the twelve-pulse rectifier, the first harmonic component in the primary side (i_A) is of 11^{th} order, and it improves the THD in inverter output voltage (v_{An}) and current (i_A). It also decreases the losses in the inductive power line. The performance parameters tabulated in Table IV indicate that the THD of the inverter output voltage and current is below 7%.

In Fig. 6b, the line-line voltages of all three phases are shown along with the line current of phase-a. It validates the balanced nature of the 3 ϕ HFAC system while feeding the non-linear load.

Inductor voltage (v_L) and current (i_L) waveforms are shown in Fig. 6c. Also, the maximum value of the peak-to-peak inductor ripple obtained from analysis, simulation and experiment are tabulated in Table V. It can be observed that the analytical model slightly overestimated the peak-to-peak ripple. This could be because the assumption that the voltage across C_f is approximately constant during the switching period may not be true as the fundamental and switching frequency are not far apart for the given problem. However, the predicted values from simulation and analysis are close, and it validates the design of filter inductor L_f.

TABLE IV
Performance Parameters of 3ϕ HFAC Inverter

P	$v_{an(pk)}$	$i_{a(pk)}$	THD(v_{an})	THD(i_{inv})
960 W	28.53 V	21.57 A	5.78%	6.54%

TABLE V
Ripple in Inductor Current (Δi_L)

Analytical	Simulation	Experiment
6.66 A	5.97 A	5.56 A

VI. Conclusion

This paper proposes a three-phase (3ϕ) high-frequency AC (HFAC) power distribution system for satellite power applications. An LTSpice simulation is performed to obtain the losses of the devices. Based on the losses and several performance parameters, a suitable device is selected, and its corresponding gate driver circuitry is designed. For sine-triangle modulation, the filter inductor (L_f) is designed to limit the ripple within 30% of the fundamental peak component. The filter capacitor is designed to restrict the voltage ripple around 2% of the fundamental peak. A brief description of the prototype development of the power board is given, and some crucial design aspects are highlighted. The experiment

is performed to validate the design approach. It is observed that both voltage and current THD are below 7%. It validates the efficacy of the proposed topology and the corresponding design approach.

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